ABSTRACT

The cache memory in the present invention is a cache entry having, in a correspondence with a cache entry which holds a data unit of caching, a valid flag indicating whether or not the cache entry is valid, and a dirty flag indicating whether or not the cache entry has been written into. The cache memory in the present invention includes an altering unit which, based on an instruction from a processor, sets, in the cache entry, an address serving as a tag and sets the valid flag, without loading data from a memory, or resets the dirty flag in a state in which the cache entry holds rewritten data that has not been written back.